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Enclosed for filing is the patent application of Inventor:  
MARC DURANTON

FOR: DATA PROCESSING ARRANGEMENT AND MEMORY SYSTEM

**ENCLOSED ARE:**

- ☒ Appointment of Associates;  
☐ Information Disclosure Statement, Form PTO-1449 and copies of documents listed therein;  
☐ Preliminary Amendment;  
☒ Specification (11 Pages of Specification, Claims, & Abstract);  
☒ Declaration and Power of Attorney:  
(2 Pages of a ☐ fully executed ☒ unsigned Declaration);  
☒ Drawing (4 sheets of ☐ informal ☒ formal sheets);  
☐ Certified copy of application Serial No.  
☒ Authorization Pursuant to 37 CFR §1.136(a)(3)  
☐ Other: ;  
☐ Assignment to

**FEE COMPUTATION**

CLAIMS AS FILED				
FOR	NUMBER FILED	NUMBER EXTRA	RATE	BASIC FEE - \$760.00
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Independent Claims	3 - 3 =		X \$78 =	
Multiple Dependent Claims, if any			\$260 =	
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☒ Amend the specification by inserting before the first line as a centered heading --Cross Reference to Related Applications--; and insert below that as a new paragraph --This is a continuation-in-part of application Serial No. 09/282,325, filed March 31, 1999, which is herein incorporated by reference--.

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09/31/99  
05/24/99

## "DATA PROCESSING ARRANGEMENT AND MEMORY SYSTEM"

### FIELD OF THE INVENTION

The present invention concerns a data processing arrangement comprising a first processor for providing successive sets of input data, a second processor for receiving successive sets of output data and a memory system comprising a plurality of memory circuits for receiving the successive sets of input data and providing the successive sets of output data.

The invention also relates to a memory system, which may receive data and provide data to several processors, and to a method of processing data carried out in such a data processing arrangement. The invention is particularly relevant for applications related to Multimedia involving streams of data.

### BACKGROUND ART

The American patent N°4,930,066 discloses a memory system comprising a plurality of data input/output ports for providing page addresses, a plurality of memory banks for storing pages of data and a switching network for rotating connections between the data input/output ports and the memory banks. An address is transmitted to the memory system in association with the data. The described system comprises therefore, for each input/output port an interface for receiving the data and the associated address. This results in delays when storing data. Moreover this interface is complex in terms of hardware. Besides a memory bank is accessible for either reading or writing but not both. A memory access conflict may occur when a memory bank is selected for both receiving a data to be written and providing a data to be read. The configuration described here is prone to conflicts when two different ports need to access two pages located in the same bank.

### SUMMARY OF THE INVENTION

It is an object of the invention to provide a data processing arrangement as defined in the opening paragraph that allows a greater simplicity.

According to the invention, such a data processing arrangement comprises a master controller for setting up the memory system by means of control commands, associated with a set of input data and a set of output data, and the memory system further comprises a control unit for, on the basis of the control commands, selecting a first memory circuit and generating a write-address in said first memory circuit when a data from the set of input data is provided by the first processor, and for, on the basis of the control commands, selecting a second memory circuit and generating a read-address in said second memory circuit when a data from the set of output data is required by the second processor.

The control commands, which are associated with a set of input data and a set of output data, set up the memory system so that it autonomously generates addresses for the

data of the two sets. The control unit in the memory system calculates internally these addresses of the input and output data and selects itself a memory circuit for each data. Thus, there is no need for a processor to transmit addresses for providing or receiving data. In fact, a processor does not need to know anything from the internal behaviour of the memory system when it requires or provides sets of data. As a result, any communication protocol that may exist between a processor and such a memory system and the resulting hardware implementation are greatly simplified comparing to the prior art.

Another advantage of the invention relates to the following aspects. In a data processing arrangement in accordance with the invention, the memory system may receive an input data from the first processor and, at the same time, it may provide an output data to the second processor. The control unit allows to counter access conflicts by selecting two different memory circuits for the input and output data. This prevents that stored data are corrupted. A memory circuit may, also, be of a type which allows, at a given instant, either reading or writing but not both. Such memory circuits are relatively cheap and thus another advantage of the invention is cost-efficiency.

The read and write-addresses may be generated in different ways. A possible way of getting these addresses is to load lookup tables with all the addresses associated with the set of input data and the set of output data. These lookup tables are, however, complex to implement and require a great chip area.

A preferred embodiment of the present invention, claimed in claim 2, comprises a read counter and a write counter for generating the read and write addresses, which determine where a data is to be stored or taken, respectively. Those two counters are a simple implementation of means for providing the read-address and write-address.

There also various manners for the memory system to know when a data from the set of input data is provided by the first processor and when a data from the set of output data is required by the second processor. A solution may be that the two counters mentioned hereinbefore count on unit up or down in response to the clock pulse of a clock signal. This implies that the input and output data are received or provided at the fixed rate determined by the clock signal.

Another embodiment of the invention claimed in claim 3, introduces a read and a write-signal from the processors. A processor sends a read or a write-signal to the memory system when it requires a new output data or when it provides a new input data. These signals allow the processors to receive or provide data asynchronously. In this embodiment of the data processing arrangement, the two processors can access the memory system at their own speeds. This is particularly advantageous if various processors have their own processing speeds and, in this case, if they cannot receive or provide data at the same rate. Comparing to the solution where the data are transmitted in response to a clock signal, the embodiment as claimed in claim 3 has the main advantage of greater flexibility.

The invention also relates to a memory system comprising a plurality of memory circuits for receiving successive sets of input data and for providing successive sets of output data, wherein the memory system further comprises a control unit being programmable by means of control commands associated with a set of input data and a set of output data and, on the basis of these control commands, for selecting a first memory circuit and generating a write-address in said first memory circuit, when a data from the set of input data is received, and for selecting a second memory circuit and generating a read-address in said second memory circuit, when a data from the set of output data is provided. The invention more generally concerns a method of processing data that is, possibly, carried out in the claimed data processing arrangement.

#### BRIEF DESCRIPTION OF THE DRAWINGS

The particular aspects of the invention will now be explained with reference to the embodiments described hereinafter and considered in connection with the accompanying drawings, in which:

- Fig.1 is a block diagram of an embodiment of a data processing arrangement in accordance with the present invention.
- Fig.2 is a block diagram of a preferred embodiment of a data processing arrangement in accordance with the invention;
- Fig.3 is a block diagram of a memory system showing the internal connections among its various components;
- Fig.4 depicts the 8-bits word MC\_W.

#### DETAILED DESCRIPTION OF THE INVENTION

A data processing arrangement 1, in accordance with the invention, is shown in Fig.1. It comprises a memory system 2, a first processor PROC1 for providing successive sets of input data to the memory system 2 and a second processor PROC2 for receiving successive sets of output data from the memory system 2. PROC1 provides a data  $D_i$  through a crossbar 6 and an input port 3 of the memory system 2. PROC2 receives a data  $D_o$  through a crossbar 5 and an output port 4 of the memory system 2. The memory system 2 comprises a memory control unit MCU and a memory block MB. This memory block MB, where data are physically stored, is composed of an arbitrary number, five here, of independent memory circuits MEM1, MEM2, MEM3, MEM4 and MEM5. These memory circuits may, in a preferred embodiment of the invention, for example be SRAM (Static Random Access Memory) of 256 words of 10 bits. Each memory circuit MEM1,...,MEM5 is accessible, when a data  $D_i$  has to be written into it, through a respective input port I1, I2, I3, I4 or I5 and is accessible, when data  $D_o$  has to be read from it, through a respective output port O1, O2, O3, O4 or O5.

The data processing arrangement 1 further comprises a master controller MCP, which through a control bus CB transmits control commands CC to the control unit MCU. These control commands CC are associated with a set of input data received from PROC1, which have to be written in the memory block MB. These control commands are also associated with a set of output data required by PROC2 and which have to be taken from the memory block MB. The commands CC are transmitted to the control unit MCU before the process of the set of input data and the process of the set of output data by PROC1 and PROC2, respectively. The commands CC operate a setup of the control unit MCU. The control unit MCU has for main function in the memory system 2, the management of the storing of data within the memory block MB. In response to these control commands, the unit MCU is able to generate a set of commands COM transmitted to the memory block MB, indicating where to take a data Do from MB or where to put a data Di into MB. Thus, when a data Di is provided in port 3 by PROC1 for being written, the MCU transmits to the memory system 2 the set COM indicating, firstly, in which memory circuit MEM1, MEM2, MEM3, MEM4 or MEM5 the data Di has to be written by activating the corresponding input port I1, I2, I3, I4 or I5. This set COM also comprises a write-address, where the data has to be written in the selected memory circuit. Similarly, when a data Do is required by PROC2 at the output port 4, the MCU sends a set COM indicating to the memory block MB which memory circuit MEM is selected and comprising a read-address within this memory circuit, where the required data is to be taken from.

It is to be noted that a write and a read operation cannot be performed simultaneously in the same memory circuit. Indeed, in order not to corrupt data that are required simultaneously for reading and writing, both operations are not allowed at the same time. When a same memory circuit is selected for simultaneous reading and writing, the read operation is inactivated and the write operation is performed normally. Simultaneous read and write operations can only be performed in two different memory circuits. As a result access conflicts are resolved in a data processing arrangement in accordance with the invention. It will be shown in further detail in a paragraph hereinafter, how access conflicts, that may occur are detected and avoided.

The memory block may be used in association with several processors. However two processors can not simultaneously access the memory system 2 for writing. Several units may, however simultaneously access the memory block MB for reading a same set of data through 4. A memory block, such as described here, is often used as a buffer memory between two processors in a processing chain.

In a preferred embodiment of the invention, the control unit MCU, shown in Fig.2, transmits the set of commands COM composed of four signals: MS, R/W, AD\_W and AD\_R. Besides, in this preferred embodiment, the control unit MCU comprises a controller CTRL, which after setup by means of the control commands CC, transmits, when a data is to be read or written, the signal MS to the memory block MB. This signal MS transmitted allows

the selection of a memory circuit MEM1, MEM2, MEM3, MEM4 or MEM5. The controller CTRL further transmits to the memory block MB the R/W signal, which indicates whether the selected memory circuit is required for reading or writing and, which allows the activation of its input port I1,..., I5 or output port O1,..., O5 depending whether the memory circuit is selected for reading or writing. This signal may for example be 1 when the selected memory circuit is required for writing and 0, when it is required for reading.

The memory control unit MCU further comprises two internal counters CNT\_R and CNT\_W, that can be externally loaded. The value of the counter CNT\_W is modified in response to a signal NXT\_W received through a write-input port 7 of the control unit MCU and provides the signal AD\_W, which is the read-address of the data Di to be written in the memory circuit selected by the controller CTRL. Thus, when the processor PROC1 provides Di, it also sends the signal NXT\_W through the crossbar 6 and the write-input port 7. Di is written in the memory circuit selected by the controller CTRL at the location within this memory circuit indicated by AD\_W. The counter CNT\_W is then incremented in response to NXT\_W and is ready to provide a new address AD\_W indicating the next available location for a next data Di provided by PROC1. The signal NXT\_W permits therefore to increment the addresses within the selected memory circuit for a continuous and asynchronous writing of the data of Di. The counter CNT\_W is, in this embodiment of the invention, incremented after the data is written into the selected memory circuit. CNT\_W may also be decremented in response to NXT\_W and before the data is written.

In the same way, when PROC2 requires a new data Do from the memory block MB, it sends a signal NXT\_R through the crossbar 5 and a read-input port 8 of the control unit MCU to the counter CNT\_R. The counter CNT\_R, in response to NXT\_R increments and provides a read-address AD\_R to MB. This address AD\_R is the address of the data Do required by PROC2 within the memory circuit selected for reading by the controller CTRL. The counter CNT\_R is incremented before the data is taken from the selected memory circuit. In an embodiment of the invention, the signals NXT\_W and NXT\_R are provided to the respective clock inputs of the counters and function therefore as asynchronous clocks for the counters CNT\_W and CNT\_R, respectively. A main advantage of this preferred embodiment is the asynchronous behaviour of the data processing arrangement 1, allowing the memory system to be accessed by processors of different processing speed. In a possible implementation of the invention the two counters are connected to a clock signal and provide, for example, the read and write-addresses at each rising edge of the clock signal. This implementation requires a synchronous behaviour of the processors, which have to receive and provide data at the fixed frequency of the clock.

An improved embodiment of the invention is depicted in Fig.3. It is shown a memory control unit MCU comprising the two counters CNT\_W and CNT\_R of Fig.2. The controller CTRL described in Fig.2 is, in this improved embodiment of the invention, composed of two internal separate controllers CTRL\_W, CTRL\_R and a separate unit COMP for detecting and

solving the access conflicts that may occur within the memory system 2. The control unit MCU is also constituted of four registers REG1, REG2, REG3 and REG4. These registers receive the set of control commands CC from the master controller MCP. This set CC is here constituted of four main command words: Strt\_W, MC\_W, MC\_R and Strt\_R. The commands MC\_W and MC\_R are stored in REG2 and REG3, respectively, in response to a load signal Id\_conf transmitted on the control bus CB from the master controller MCP. Strt\_W and Strt\_R are loaded in REG1 and REG4, respectively, in response to a Id signal from the controllers CTRL\_W and CTRL\_R, respectively. The content of REG1 is transmitted to the counter CNT\_W via a connection line 10. The content of REG2 is transmitted to the controller CTRL\_W via a connection line 11. The content of REG3 is transmitted to the controller CTRL\_R via a connection line 12. And the content of REG4 is transmitted to the counter CNT\_R via a connection line 13. This Id\_conf signal, transmitted on the control bus CB, activates the setup of the memory control unit MCU. Indeed, in response to this signal Id\_conf the contents of the registers REG2, REG3 are updated with the new control commands CC received on the control bus CB.

The memory block shown in Fig.3 is symmetrical considering that an upper part of the memory block concerns the write function of the memory block and that a symmetrical lower part concerns the read function of the memory block. The description hereinafter is mainly focused on the elements of the memory block related to the write function but what is said for these elements is also valid for the symmetrical elements related to the read function.

Strt\_W, MC\_W, MC\_R and Strt\_R may be 8-bits words for which the bits have the meanings described hereinafter. The signals MC\_R and MC\_W, respectively, define a read pattern for a read processing cycle and a write pattern for a write processing cycle. A processing cycle starts with a new set of control commands CC loaded in the controllers CTRL\_W, CTRL\_R during the setup phase. The exact meaning of each bit in the 8-bits word MC\_W, shown in Fig.4, is explained as follows:

- The least significant bit, MC\_W[0], indicates if a write operation is enabled. When this bit is set to "1", the write operation is allowed, when set to "0", the write operation is inactivated, the counter CNT\_W is not incremented and the other bits of MC\_W are ignored.
- MC\_W[1] and MC\_W[2] select the write operation pattern among four possible patterns. Table 1 defines a code memorized in the internal controller CTRL\_W that gives a pattern for the write operation.

MC_W[2]	MC_W[1]	Write pattern
0	0	Reset of CNT_W (i.e. AD_W=8b0) via line 14
0	1	Start the write operation from the address given by Strt_W, loaded in REG1 in response to the signal Id from CTRL_W
1	0	Continue the write operation from the current address,

		including the current memory circuit
1	1	Continue from the current address and from the memory circuit indicated by MC_W[3], MC_W[4] and MC_W[5]

Table 1

- MC\_W[3], MC\_W[4] and MC\_W[5] indicate the value of the starting memory circuit number for writing during the writing cycle. In this embodiment of the invention the memory block MB comprises five independent memory circuits, the number of a memory circuit, which goes from 1 to 5, is in this case binary encoded in 3 bits.

- MC\_W[6] is unused.

- The most significant bit, MC\_W[7], indicates a need for change in the memory circuit number during the write cycle. When this bit is set to "0" then the memory circuit number is automatically incremented when the 8-bits address counter CNT\_W goes from the beginning of a memory circuit to the end. If the memory circuit number is equal to the maximum, here 5, then the memory circuit number, coded in MC\_W[3], MC\_W[4] and MC\_W[5] is set to 1. The controller CTRL\_W has access to the current value of CNT\_W for checking through the connection line 14. When this bit is set to "1", the memory circuit number coded in MC\_W[3], MC\_W[4] and MC\_W[5] is not changed during the write cycle.

A similar description is also valid for the 8-bits word MC\_R. Its bits have the same signification as the bits of MC\_W, for a read processing cycle this time. Thus, the controller CTRL\_R checks and resets the value of CNT\_R through a connection line 17 and allow the counter CNT\_R to load a new value in response to a command Id.

An access conflict may occur when a memory circuit selected for a read operation is the same as the memory circuit selected for a write operation, i.e. MC\_W[3]=MC\_R[3]=MC\_R[3], MC\_W[4]=MC\_R[4], MC\_W[5]=MC\_R[5]. A conflict is real when, in addition, the write and read operations are both enabled, i.e. MC\_W[0]=1 and MC\_R[0]=1. The unit COMP receives from CTRL\_W the bits MC\_W[0], MC\_W[3], MC\_W[4], MC\_W[5], transmitted on 15, and from CTRL\_R the bits MC\_R[0], MC\_R[3], MC\_R[4], MC\_R[5], transmitted on 16. The unit COMP compares bit-by-bit the bits received and when it detects a real memory access conflict (the memory circuits numbers selected for reading and writing are the same and the read and write operations are both enabled) it makes, through 16, the bit MC\_R[0], which tells if the read operation is enabled, to be read as a 0 by CTRL\_R. In fact, the unit COMP does not exactly modify MC\_R[0], which stays at 1 but it makes it be read as a 0 by the controller CTRL\_R. The conflict stops either because one of the read and write operation is disabled during a new setup phase or either because the number of the memory circuit to be accessed for reading or writing is modified during a new setup or within the course of the read or write operation. In such a case the unit COMP does not detect further conflict and the write operation is performed normally.



Let it be considered that a data  $D_i$  needs to be written within the memory system 2.  $D_i$  is provided in port 3 and at the same time CTRL\_W and CNT\_W transmit their respective signals MS, R/W and AD\_W. The MS signal is, for example, the three coded bits representing the memory circuit number to be selected. This signal is transmitted to a demultiplexer DEMUX, whose outputs are connected to each memory circuit MEM. The demultiplexer DEMUX transmits a 1 to the memory circuit, whose number is coded in MS and transmits a 0 to all the other memory circuits. The R/W signal is transmitted to all the memory circuits but is only taken into account by the selected memory circuit and also results in the activation of the input port of the memory circuit for the writing of  $D_i$ . The write-address AD\_W is, as well, transmitted to all the memory circuits but, again, is only taken into account by the selected memory circuit. The data is then transmitted in the memory block towards the activated input port and to the indicated location within the selected memory circuit.

In an ameliorated embodiment of the invention, the memory system 2 may send a signal to indicate to the processors if it is ready to receive or provide data. This would prevent a processor to access the memory for reading when it is empty or for writing when it is already full.

The drawings and their description hereinbefore illustrate rather than limit the invention. It will be evident that there are numerous alternatives which fall within the scope of the appended claims. In this respect, the following closing remarks are made.

There are numerous ways of physically spreading functions or functional elements over various units. In this respect, the drawings are very diagrammatic, each representing only one possible embodiment of the invention. Thus, although a drawing shows different functional elements or all functional elements as a single physical unit.

## CLAIMS

1. A data processing arrangement (1) comprising:
  - a first processor (PROC1) for providing successive sets of input data;
  - a second processor (PROC2) for receiving successive sets of output data;
  - a memory system (2) comprising a plurality of memory circuits (MEM) for receiving the successive sets of input data and providing the successive sets of output data,
 wherein
  - the data processing arrangement further comprises a master controller (MCP) for setting up the memory system by means of control commands (CC) associated with a set of input data and a set of output data;
  - the memory system further comprises a control unit (MCU):
    - for, on the basis of the control commands, selecting a first memory circuit and generating a write-address (AD\_W) in said first memory circuit when a data (Di) from the set of input data is provided by the first processor, and
    - for, on the basis of the control commands, selecting a second memory circuit and generating a read-address (AD\_R) in said second memory circuit when a data (Do) from the set of output data is required by the second processor.
2. A data processing arrangement, as claimed in claim 1, wherein the control unit comprises:
  - a write-counter (CNT\_W) whose value is modified in association with a data received from the set of input data and which value indicates the write-address of the data in said first memory circuit;
  - a read-counter (CNT\_R) whose value is modified in association with a data provided from the set of output data and which value indicates the read-address of the data in said second memory circuit.
3. A data processing arrangement, as claimed in claim 1, wherein the control unit comprises a write-input port (7) for receiving a write-data signal (NXT\_W) from the first processor in response to which the control unit generates the write-address and the control unit further comprises a read-input port (8) for receiving a read-data signal (NXT\_R) from the second processor in response to which the control unit generates the read-address.
4. A memory system (2) comprising a plurality of memory circuits (MEM) for receiving successive sets of input data and for providing successive sets of output data, wherein the memory system further comprises a control unit (MCU) being programmable by means of control commands (CC) associated with a set of input data and a set of output data and, on the basis of these control commands, for selecting a first memory circuit and generating a

write-address (AD\_W) in said first memory circuit, when a data (Di) from the set of input data is received, and for selecting a second memory circuit and generating a read-address (AD\_R) in said second memory circuit, when a data (Do) from the set of output data is provided.

5. A method of processing data in a data processing arrangement (1) comprising:
  - a first processor (PROC1) for providing successive sets of input data;
  - a second processor (PROC2) for receiving successive sets of output data;
  - a memory system (2) comprising a plurality of memory circuits (MEM) for receiving the successive sets of input data and providing the successive sets of output data, wherein the method comprises, for a set of input data and a set of output data, the following steps:
    - a configuration step in which the memory system is set up by means of control commands associated with the set of input data and the set of output data;
    - an execution step in which, on the basis of the control commands, the memory system:
      - selects a first memory circuit and generates a write-address in the first memory circuit for a data belonging to the set of input data;
      - selects a second memory circuit and generates a read-address in the second memory circuit for a data belonging to the set of output data.

"Data processing arrangement and memory system"

A data processing arrangement (1) comprises a first processor (PROC1) for providing successive sets of input data, a second processor (PROC2) for receiving successive sets of output data and a memory system (2) comprising a plurality of memory circuits (MEM) for storing the input and output data. According to the invention, the data processing arrangement further comprises a master controller (MCP) for setting up the memory system by means of control commands (CC) associated with a set of input data and a set of output data. These control commands are received in the memory system by a control unit (MCU). When a data (Di) from the set of input data is provided by the first processor, this control unit selects, on the basis of the control commands, a first memory circuit and generates a write-address (AD\_W) in said first memory circuit. In the same way, when a data (Do) from the set of output data is required by the second processor, the control unit, on the basis of the control commands, selects a second memory circuit and generates a read-address (AD\_R) in said second memory circuit. Thus, there is no need for the processors to provide addresses when they require or send data therefore leading to a simple data processing arrangement.

634400-092426

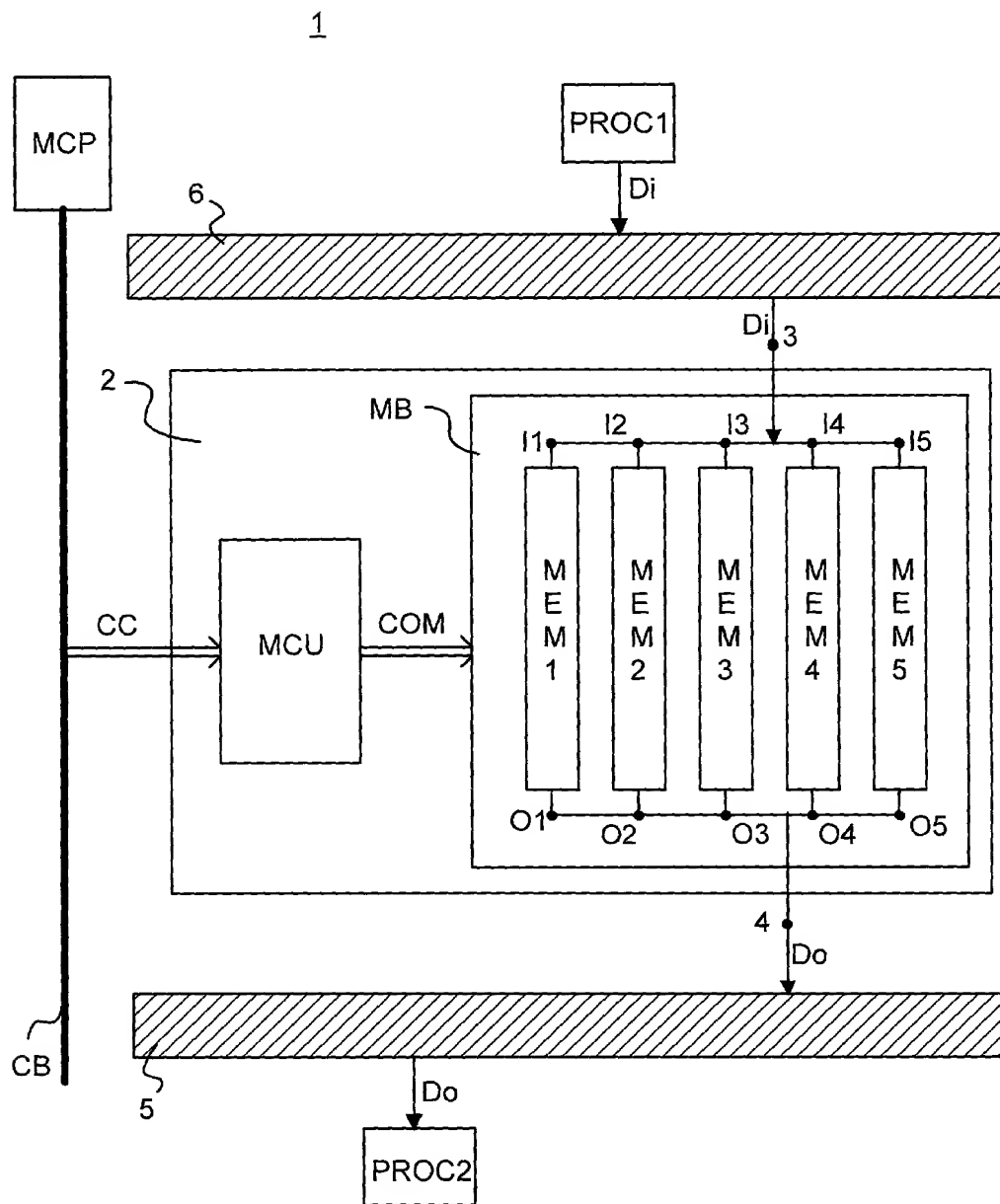


FIG.1

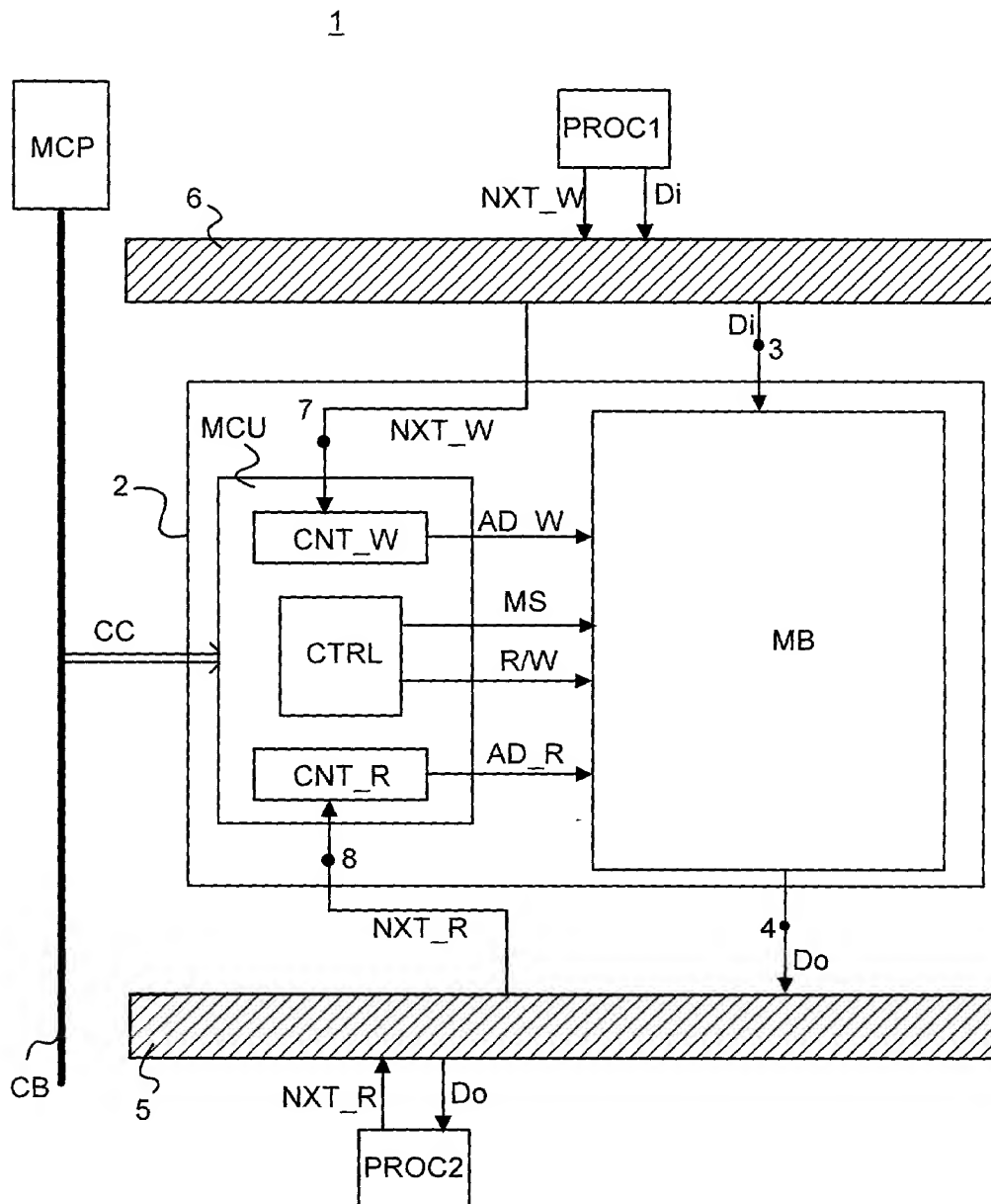


FIG.2

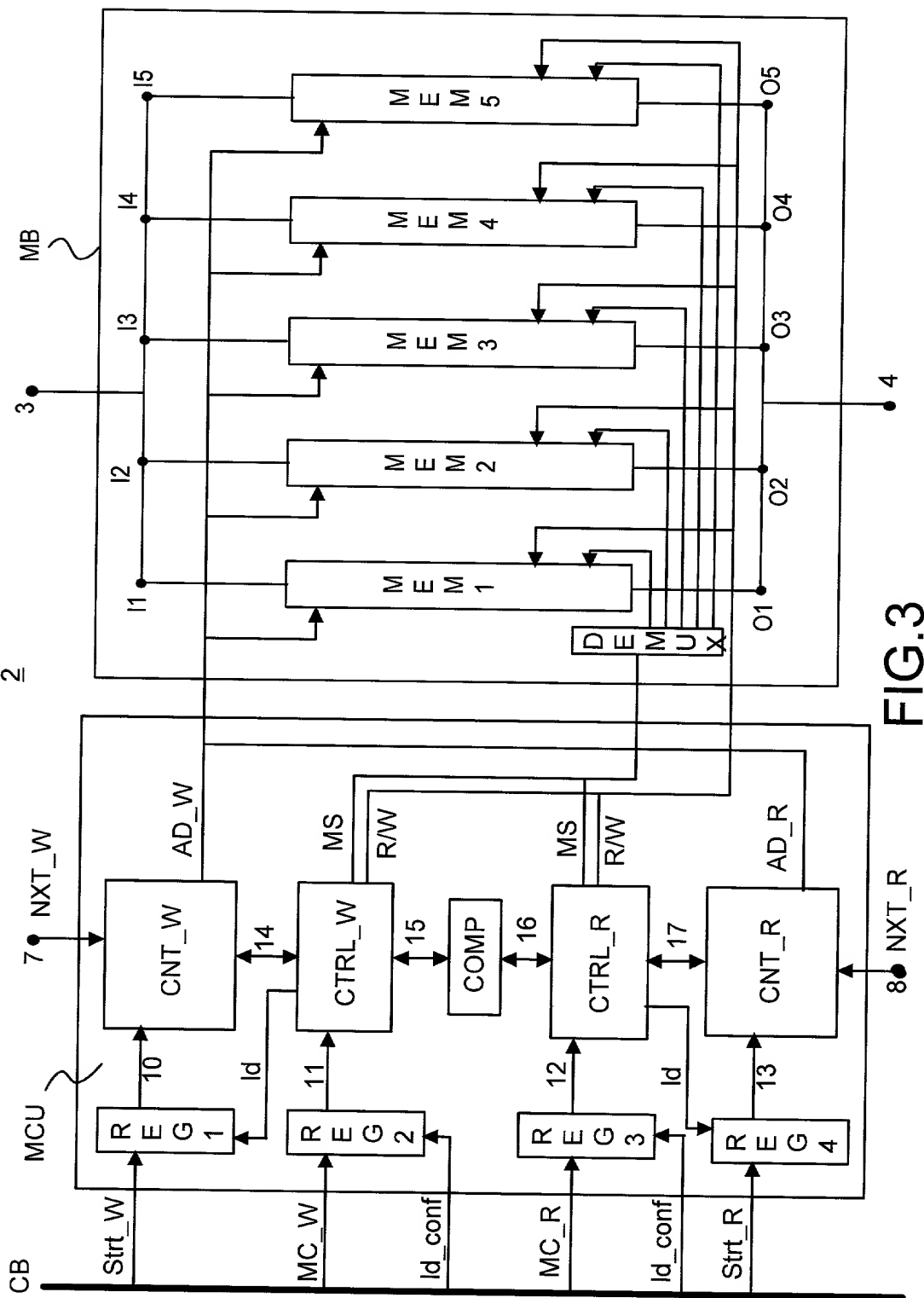


FIG.3

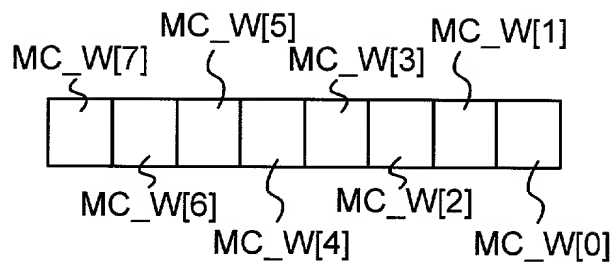


FIG.4



# DECLARATION and POWER OF ATTORNEY

Attorney's Docket No.

PHF 99,540V

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled DATA PROCESSING ARRANGEMENT AND MEMORY SYSTEM

the specification of which (check one)

XXX is attached hereto.

was filed on \_\_\_\_\_ as Application Serial No. \_\_\_\_\_ and was amended on \_\_\_\_\_ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by the amendment(s) referred to above.

I acknowledge the duty to disclose information which is material to the patentability of this application in accordance with Title 37, Code of Federal Regulation, §1.56(a).

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

## PRIOR FOREIGN APPLICATION(S)

COUNTRY	APPLICATION NUMBER	DATE OF FILING (DAY, MONTH, YEAR)	PRIORITY CLAIMED UNDER 35 U.S.C. 119

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35 United States Code, §112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, §1.56(a) which occurred between the filing date of the prior application and the national or PCT international filing date of this application:

## PRIOR UNITED STATES APPLICATION(S)

APPLICATION SERIAL NUMBER	FILING DATE	STATUS (PATENTED, PENDING, ABANDONED)
09/282,325	MARCH 31, 1999	PENDING

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

**POWER OF ATTORNEY:** As a named inventor, I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. (list name and registration number)

Algy Tamoshunas, Reg. No. 27,677

Jack E. Haken, Reg. No. 26,902

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Dated:		INVENTOR'S SIGNATURE:		
Full Name of Inventor	Last Name DURANTON	FIRST NAME MARC	Middle Name	
Residence & Citizenship	City 94470 BOISSY SAINT LEGER	STATE OR FOREIGN COUNTRY FRANCE	Country of Citizenship FRANCE	
Post Office Address	Street 24, RUE DE PARIS	CITY 94470 BOISSY SAINT LEGER	State or Country FRANCE	Zip Code 94470

Dated:		INVENTOR'S SIGNATURE:		
Full Name of Inventor	Last Name	FIRST NAME	Middle Name	
Residence & Citizenship	City	STATE OR FOREIGN COUNTRY	Country of Citizenship	
Post Office Address	Street	CITY	State or Country	Zip Code

Dated:		INVENTOR'S SIGNATURE:		
Full Name of Inventor	Last Name	FIRST NAME	Middle Name	
Residence & Citizenship	City	STATE OR FOREIGN COUNTRY	Country of Citizenship	
Post Office Address	Street	CITY	State or Country	Zip Code

Dated:		INVENTOR'S SIGNATURE:		
Full Name of Inventor	Last Name	FIRST NAME	Middle Name	
Residence & Citizenship	City	STATE OR FOREIGN COUNTRY	Country of Citizenship	
Post Office Address	Street	CITY	State or Country	Zip Code

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE  
In re Application of Atty. Docket  
MARC DURANTON PHF 99,540V

Serial No.

Filed: CONCURRENTLY

DATA PROCESSING ARRANGEMENT AND MEMORY SYSTEM

Honorable Commissioner of Patents and Trademarks  
Washington, D.C. 20231

APPOINTMENT OF ASSOCIATES

Sir:

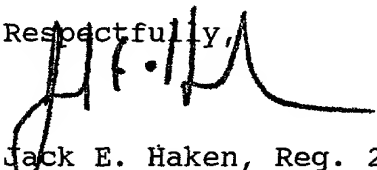
The undersigned Attorney of Record hereby revokes  
all prior appointments (if any) of Associate Attorney(s) or  
Agent(s) in the above-captioned case and appoints:

**Laurie E. Gathman** (Registration No. 37,520)

c/o U.S. PHILIPS CORPORATION, Intellectual Property  
Department, 580 White Plains Road, Tarrytown, New York  
10591, his Associate Attorney(s)/Agent(s) with all the usual  
powers to prosecute the above-identified application and any  
division or continuation thereof, to make alterations and  
amendments therein, and to transact all business in the  
Patent and Trademark Office connected therewith.

ALL CORRESPONDENCE CONCERNING THIS APPLICATION AND  
THE LETTERS PATENT WHEN GRANTED SHOULD BE ADDRESSED TO THE  
UNDERSIGNED ATTORNEY OF RECORD.

Respectfully,

  
Jack E. Haken, Reg. 26,902  
Attorney of Record

Dated at Tarrytown, New York  
on May 21, 1999.